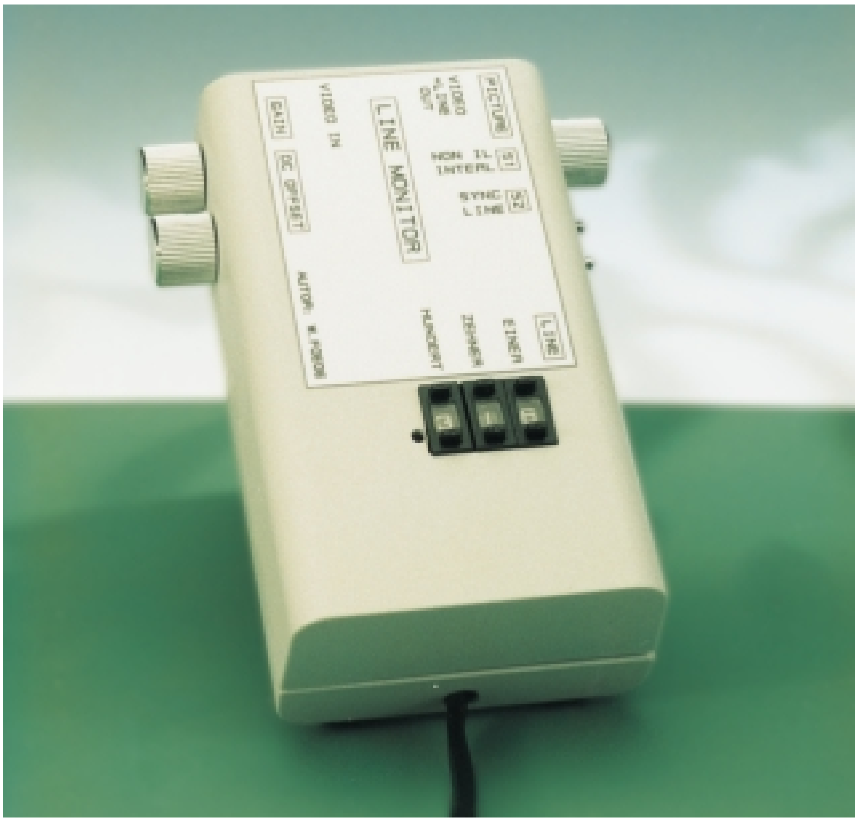
# enhanced TV line monitor

## select and check video line contents

The tester presented here can do more than just generate an oscilloscope trigger pulse for a selected video raster line. It also marks the selected line in the CVBS signal and displays it on the TV screen as an oscillogram.



Design by W. Foede

### Features:

- ✓ *exact selection of one horizontal line (1 through 625)*
- ✓ *oscilloscope trigger output*
- ✓ *selected line marked in the passed-through video signal*
- ✓ *oscillogram of the selected line merged with the television picture; amplitude and position adjustable*
- ✓ *adjustable blend of original picture and oscillogram*
- ✓ *line content displayed either aligned to picture or offset with a horizontal sync pulse*
- ✓ *interlaced and non-interlaced operating modes*

In order to be able to display a given line of a video image on an oscilloscope, you need a special trigger generator that uses the vertical synchronization pulse to detect the start of the frame or field (half frame) and then counts horizontal sync pulses until the desired line is reached, whereupon it generates a trigger pulse for the oscilloscope.

A circuit which does this (and only this) was published in the October 1994 issue of *Elektor Electronics* (‘TV Line Monitor’). In that circuit, a microcontroller looks after all the counting and control tasks — everything except for sync separation. However, at the cost of only a little more hardware, this basic

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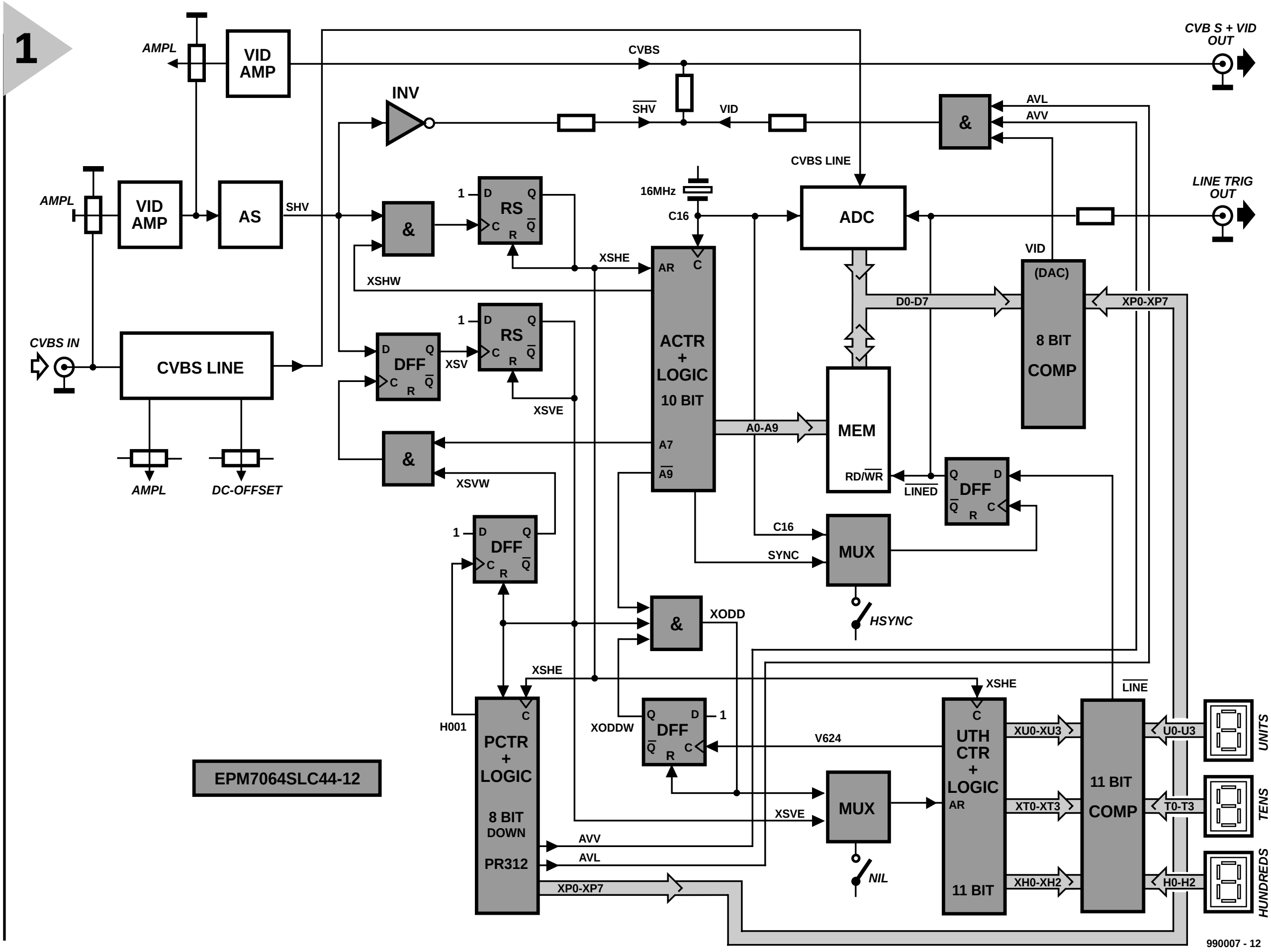

***Figure 1. Block diagram of the enhanced TV line monitor. The shaded elements are contained in a ready-programmed EPLD IC.***

function can be enhanced with a number of interesting extras (see the 'Features' box). Since this tester evaluates not only the sync pulses but also the content of the selected line, a different approach must be taken.

The video signal follows two different paths from the input. The first path leads to a video amplifier built using discrete components, in which the sync pulses are separated from the video signal so that they can be used to trigger the line counter. The second path is digital. First the CVBS (composite video) signal is sampled by an A/D converter, and the resulting data are stored in a fast RAM. A D/A converter restores the selected line to analogue form and merges it with the amplified CVBS signal in an output buffer amplifier. The enhanced TV line monitor also offers a range of operational settings, and it produces the external trigger signal that is essential for making measurements with an oscilloscope.

## ANALOGUE AND PROGRAMMABLE LOGIC

The block diagram of the TV line monitor, shown in **Figure 1**, is fairly elaborate. The shaded elements are located in a programmable EPLD IC (Altera type EPM7064). A smaller version of this IC has already been used in several *Elektor Electronics* projects. Here this IC has three principal functions: it counts sync pulses, it controls the input A/D converter and RAM, and finally it looks after the conversion of the stored line back into analogue form. Let's look at the various elements of the block diagram in more detail.

### CVBS LINE

The first item that the input video signal encounters is labelled 'CVBS LINE'. This is actually just a few passive components, as can be seen from the otherwise not particularly informative schematic diagram shown in **Figure 2**. The amplitude of the input signal can be adjusted with P1, while P3 adds a d.c. component to the signal. Diode D2 and capacitor C7 clamp the sync impulses to a constant d.c. level. After this processing, the signal arrives at the A/D converter IC, a National Semiconductor ADC1175CIJM. This has an input range of +0.6 V to +2.6 V.

### VID AMP and AS

The two-stage video amplifier (T2 and T3) is also connected to the input. It raises the amplitude of the video signal by at most a factor of around 2. The input impedance has been modified to be 125 Ω instead of the usual 75 Ω, to provide satisfactory operation with input voltages lower than 1 $V_{pp}$. If on the other hand the input voltage is too high, overloading of the amplifier can be prevented by adjusting the level control P4. Sync pulses are clamped by D1 and C2.

The block labelled 'AS' contains a low-pass filter (R9/C8) that blocks HF components, such as the burst and chrominance signals.

T4 generates positive vertical and horizontal sync pulses with an amplitude of 5 $V_{pp}$ (signal SHV).

## COUNTING IN WINDOWS

The SHV signal contains all the information that the programmed logic needs in order to generate the necessary clock and reset signals (XSHE, XSHV and XODD) for the three counters programmed into the EPM7064. All of these signals, by the way, pass through edge detectors which convert them into 'needle' pulses.

### Pixel counter

The binary pixel counter, labelled 'ACTR', addresses the RAM for both reading and writing. It is 10 bits wide

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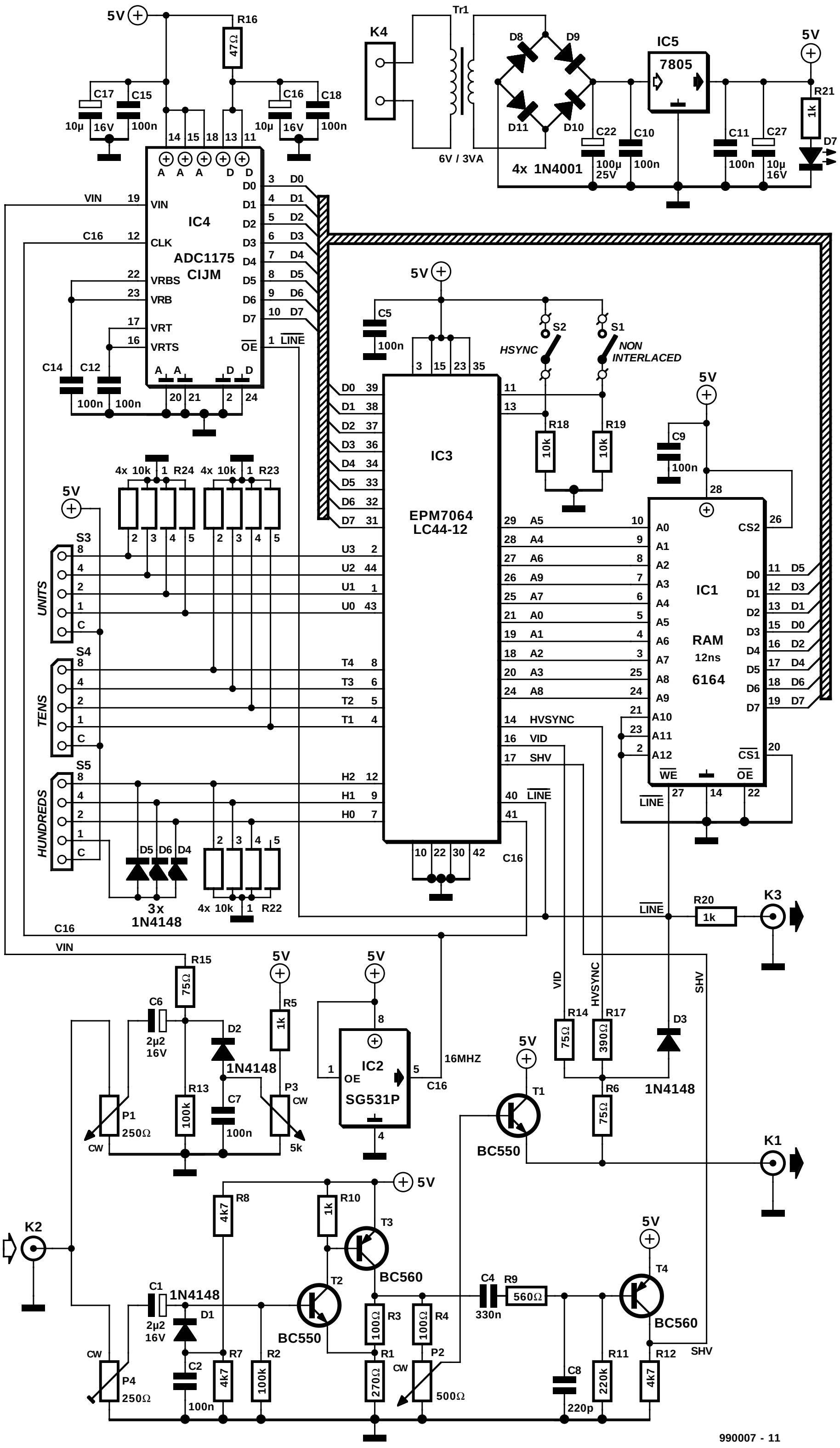

*Figure 2. Schematic diagram of the enhanced TV line monitor.*

and is clocked at 16 MHz. It is reset by the leading edge of the line sync pulse XSHE. For reliable synchronisation, the ACTR logic generates an 0.5-µs time window (XSHW) for the leading edge of line sync pulse. This (as well as the other time windows) acts as effective interference suppressor. Only the leading edge of the SHV signal that occurs within the XSHW window produces the XSHE signal, which resets the ACTR and also clocks the line counter.

**Line counter**

The line counter, labelled 'PCTR', is an 8-bit binary down counter which provides the programmed-logic D/A converter with the current line number of the input video signal. In addition, PCTR provides the two signals AVV and AVL. AVV marks the region in which the merged-in line oscillogram can be displayed (in lines 60 through 275 of the first field and 372 through 587 of the second field). AVL refers to line identification (first field = lines 24 through 311, second field = lines 336 through 623). These regions must be defined to avoid upsetting the vertical synchronisation of the television set. The PCTR counter is reset by the rising

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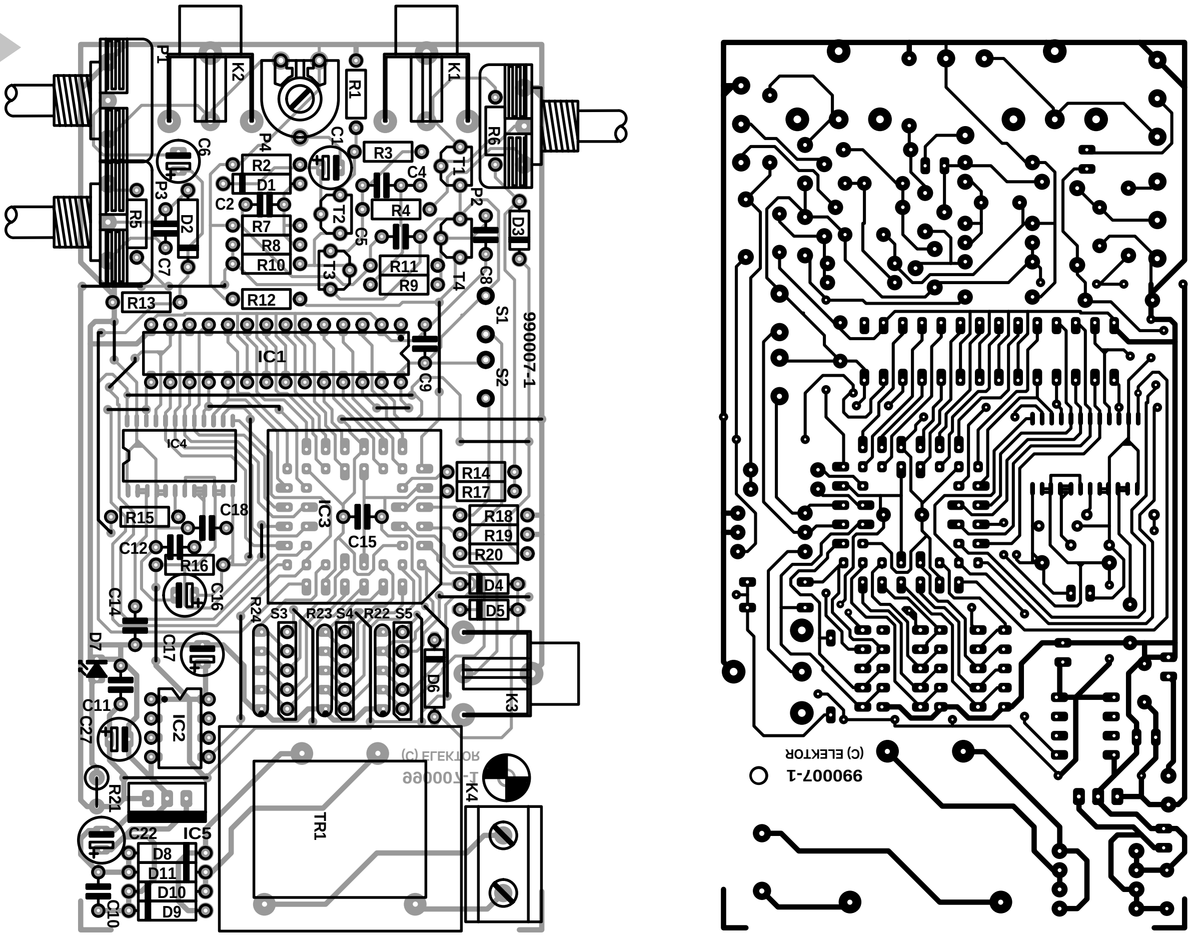

*Figure 3. Everything on one board: no internal cabling is needed.*

**COMPONENTS LIST**

**Resistors:**
R1 = 270Ω
R2,R13 = 100kΩ
R3,R4 = 100Ω
R5,R10,R20,R21 = 1kΩ
R6,R14,R15 = 75Ω
R7,R8,R12 = 4kΩ7
R9 = 560Ω
R11 = 220kΩ
R16 = 47Ω
R17 = 390Ω
R18,R19 = 10kΩ
R22...R24 = 4-way 10kΩ SIL array
P1 = 250Ω linear potentiometer
P2 = 500Ω linear potentiometer
P3 = 5kΩ linear potentiometer
P4 = 250Ω preset H

**Capacitors:**
C1,C6 = 2µF2 16V radial
C2,C5,C7,C9-C12,C14,C15, C18 = 100nF, 5mm raster
C4 = 330nF, 5mm raster
C8 = 220pF
C16,C17,C27 = 10µF 16V radial
C22 = 100µF 25V radial

**Semiconductors:**
D1-D6 = 1N4148
D7 = LED, low current
D8-D11 = 1N4001
T1,T2 = BC550
T3,T4 = BC560
IC1 = 6164
IC2 = SG531P 16MHz
IC3 = EPM7064LC44-12 (order code **986523-1**)
IC4 = ADC1175-50 CIJM SMD
IC5 = 7805

**Miscellaneous:**
K1,K2,K3 = cinch socket, PCB mount, angled (Monacor/Monarch T-709)
S1,S2 = switch, 1 make contact
TR1 = mains transformer, 6V 3VA
S3,S4,S5 = hex thumbwheel switch (RS-components o/n 199-251, sequence C-1-2-4-8)
K4 = 2-way PCB terminal block, raster 7.5mm
Enclosure 125x70x40mm (e.g. Donau SD20)
PCB, order code **990007-1**

edge of the vertical sync pulse XSVE that falls within the timing window XSVW.

**Line selector**

The block labelled 'UTHCTR' is a three-digit BCD counter that is also clocked by XSHE. The ones and tens digits have four bits each, while three bits are sufficient for the hundreds digit, since the highest possible line number is only 625. This counter is reset by the leading edge of the frame sync pulse. Depending on the setting of the mode selection switch 'NIL', this is either the XSVE pulse (non-interlaced mode, lines 1 through 312) or the XODD pulse (interlaced mode, lines 1 through 625).

The UTHCTR outputs drive a comparator whose second set of inputs is connected to three thumbwheel switches. When the current line number matches the number set in the switches, the comparator generates the $\overline{\text{LINE}}$ signal. This signal passes through a flip-flop that is clocked by ACTR (and the 16-MHz clock) such that the line to be monitored is displayed starting either at the beginning of the visible horizontal line (aligned to the TV picture) or offset by a visible synchronisation pulse, depending on the position of the HSYNC switch. The signal from the flip-flop, with appropriately modified timing, is labelled '$\overline{\text{LINED}}$'. It pro-

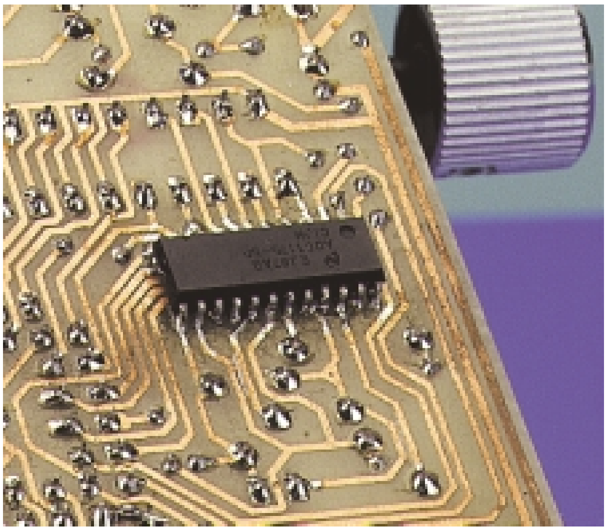

***Figure 4. The A/D converter IC is mounted on the bottom (solder side) of the board.***

vides the timing window for the A/D converter and video line memory.

**High-speed D/A converter and video line memory**

The $\overline{\text{LINED}}$ signal ensures that exactly one raster line, with a duration of 64 µs, is read, converted and stored in RAM. Since the converter is clocked at 16 MHz, 1024 samples are stored (64 µs x 16 MHz). In addition, $\overline{\text{LINED}}$ is made available at the 'LINE TRIG OUT' output socket to serve as a trigger signal for an oscilloscope.

**D/A converter**

The D/A converter ('DAC') is a 'home-brew' design. The standard polarity of the video signal is +CVBS, which means that the sync pulses have a low level and white video has a high level. The sync pulses are thus stored in the RAM as small binary values, while white regions are stored as large binary values. To obtain a correctly oriented display of the content of the stored line, the down counter ACTR must be used (high line numbers at the top of the screen and low line numbers at the bottom). The DAC is started in line 40 with a counter state of 255. The 8-bit comparator (DAC) compares the counter state for each raster line with the values provided by the line memory (MEM), which in turn is driven by ACTR in a periodic manner. It assigns the state of the PCTR counter to each digitized voltage value. For example, when the counter state is 155 (corresponding to raster line 140), every stored sample with a value of 155 generates a pixel in the VID signal. If AVV and AVL are both active, this forces the video signal to the white level. The line content diagram thus becomes part of the output signal.

**Output signals**

The output signal CVBS + VID OUT consists of the combination of the reproduced line content diagram, the CVBS signal (amplified and buffered, with adjustable amplitude) and the combined sync signal SHV. The blend of the CVBS and line content signals can be continuously adjusted with P3, starting with a colour CVBS picture with a faint oscillogram, passing through monochrome CVBS and ending with a display of the oscillogram alone without the CVBS image. The selected line is shown as a white line within the AVL region for identification.

## ALL ON ONE BOARD

After this somewhat roundabout journey through the logic of the TV line monitor, we can turn our attention to its construction. As can readily be seen from **Figure 3**, all components are mounted on one single-sided printed circuit board, including the power transformer, jacks and presets. Note however that if you want to use BNC sockets instead of the specified Cinch sockets, you will have to make a few additional short cables.

Installing the components on the board is somewhat tricky, due in part to the 22 wire jumpers. Since some of these run very close to other components, you should use fine insulated wire for all of them. Once all the jumpers have been soldered in place, mount the SMD IC before any of the other components. After this, continue in the usual manner with the low-profile components such as resistors, diodes and capacitors, and finish off with the transformer, switches S1 and S2, the jacks, presets and so on. Mount the switches elevated above the board, so that their levers will later protrude conveniently from the enclosure. By the way, C15 should be mounted either flat inside the socket or on the back (solder side) of the board. The ICs as well as the thumbwheel switches may be mounted in sockets. When soldering, take care to avoid making any solder bridges between the tracks or solder pads, which are very close together is some places.

Before putting the TV line monitor into use, you should carefully inspect the finished circuit board. Once you have verified that all polarized components (including the thumbwheel switches!) have been correctly installed, attach the mains cable to K4 and secure it with a suitable strain relief. Then attach the circuit board to the lower part of the enclosure (one screw only) and press the upper part of the enclosure into place (after first making the necessary holes and cutaways!). The two switches S1 and S2 can be left free or attached only loosely.

## PRACTICAL ASPECTS

Let's review the inputs, outputs and controls of the TV line monitor. It has a video signal input (K2, CVBS IN), which can accept a signal from a video recorder, PC video card, satellite receiver or other video source. Adjust P4 so that the strongest available video signal does not overdrive the first video amplifier stage (T2). P1 controls the amplitude of the line content oscillogram, while P2 controls its location on the screen.

The output signal leaves the TV line monitor via K2. On the connected monitor (TV), you will see the input signal (picture), a white line (the selected line) and an oscillogram of the selected line. The relative strengths of these signal can be adjusted with P3.

If you want to observe the selected line on an oscilloscope, connect the CVBS signal to the Y input and the line monitor K3 output to the external trigger input of the oscilloscope.

Since the picture contents of adjacent lines in the first and second fields are often nearly identical, the number of sampled pixels can be doubled by displaying both lines at once. To do so, set switch S1 to non-interlaced (2 x 312 lines). This operating mode also allows non-interlaced television signals to be processed, such as that produced by the Elektor Video Test Chart Generator (September and October 1996 issues). If you wish to observe only one line per frame (1 x 625 lines), S1 must be set to interlaced mode.

The function of switch S2 can best be demonstrated by trying it out with the TV line monitor in operation: the oscillogram in the CVBS output signal either includes a sync pulse, or it doesn't.

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